CLAIMS:

1. A method of fabricating a chip with an insulation layer (7) for the side walls of metal bumps (6a, 6b) with the chip comprising

- a non-conductive chip's substrate (2),
- metal pads (1a, 1b) deposited on the non-conductive chip's substrate (2),
- a passivation layer (3) covering the non-conductive chip's substrate (2) and the edges of the metal pads (1a, 1b),
- a metal diffusion stop barrier (4′) covering a portion of the chip's passivation layer (3) and the metal pads (1a, 1b),
- a photo resist pattern (5) on a metal layer (4) to expose portions of the metal layer (4) on the pad (1a, 1b) that is removed after use and
- at least one bump (6a, 6b) on the exposed portion of the pad (1a, 1b) and the edges of the metal layer (4)

characterized by the steps of

- depositing the metal layer (4) covering the chip's passivation layer (3) and the metal pads (1a, 1b),
- depositing an insulation layer (7) in a plasma activated reactor,
- removing predetermined portions of the insulation layer (7) by reactive ion etching and
- partially removing the metal layer (4) such that the remaining metal material forms the bump diffusion stop barrier (4′).

2. A connector (10) for a chip's substrate (2) and an opposite substrate (9) comprising:

- a plurality of electrode pads (8a, 8b) on the opposite substrate (9);

- a plurality of electrically conductive bumps (6a, 6b) on the chip's substrate (2), each of the electrically conductive bumps (6a, 6b) being electrically connected to a respective one of the plurality of electrode pads (8a, 8b) on the opposite substrate (9);

- a plurality of conductive particles (11) on respective top surfaces of the electrically conductive bumps (6a, 6b) electrically connecting respective electrically conductive bumps (6a, 6b) to the plurality of electrode pads (8a, 8b), and

- an insulating layer (7) formed of a nitrate or an oxide on the surfaces of the side walls of each of the plurality of electrically conductive bumps (6a, 6b) to prevent an electrical short between two bumps

characterized in that the insulation layer (7) is provided by an LPCVD-process.

3. Metal bumps (6a, 6b) that comprise side walls that are covered with an insulation layer (7) on at least two opposite side walls facing each other, characterized in that the insulation layer (7) is a dielectric layer which is formed by plasma deposition and is partially etched back in an anisotropic plasma etcher.

4. Metal bumps as claimed in claim 3, characterized in that the dielectric material is selected from the group consisting of SiO2 and Si3N4.

5. Metal bumps as claimed in claim 3 or 4, characterized in that the metal bumps (6a, 6b) are formed of a noble metal or an oxidation resistant material such as gold.

6. Use of a metal bump (6a, 6b) that is partially covered with an insulation layer (7) which is deposited by an LPCVD process for a Chip on Glass or a Chip on Foil packaging application.

7. An arrangement with a chip's substrate (2) and an opposite substrate (9) comprising:

- a plurality of electrode pads (8a, 8b) on the opposite substrate (9);
- a plurality of electrically conductive bumps (6a, 6b) on the chip's substrate (2), each of the electrically conductive bumps (6a, 6b) being electrically connected to a respective one of the plurality of electrode pads (8a, 8b) on the opposite substrate (9);
- a plurality of conductive particles (11) on respective top surfaces of the electrically conductive bumps (6a, 6b) electrically connecting respective electrically conductive bumps (6a, 6b) to the plurality of electrode pads (8a, 8b), and
- an insulating layer (7) formed of a nitrate or an oxide on the surfaces of the side walls of each of the plurality of electrically conductive bumps (6a, 6b) to prevent an electrical short between two bumps

characterized in that the insulation layer (7) is provided by an LPCVD-process.